

any



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,199	04/11/2001	Chul-min Kim	P56350	1159

7590 06/26/2006  
Robert E. Bushnell  
Suite 300  
1522 K Street, N.W.  
Washington, DC 20005-1202

EXAMINER

ONUAKU, CHRISTOPHER O

ART UNIT	PAPER NUMBER
----------	--------------

2621

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-6&16 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: steps that disclose the method claim of claims 1-6&16.

### ***Allowable Subject Matter***

3. Claims 7-23 are allowable over the prior art of record.
4. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 7, the invention relates to a video signal processing integrated circuit (IC), including a method for designing a de-emphasis circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the number of components of external application circuits of a de-emphasis output terminal of the video signal processing IC, and an IC made by the method.

The closest references Nonaka et al (US 5,872,605) disclose a video signal processing apparatus, which includes an equalizer for delaying an input color signal by

an adjustable phase retardation, made into an integrated circuit, and Kitamura et al (US 5,132,806) teach semiconductor integrated circuit devices, including techniques which are effective when applied to a semiconductor integrated circuit device for use in a color video tape recorder (VTR).

However, Nonaka et al and Kitamura et al fail to explicitly disclose a video signal processing integrated circuit, where the integrated circuit incorporates a determining circuit for determining a level of a reproduced video signal of a de-emphasis circuit, wherein the determining circuit includes a reproduced video level setting unit.

Regarding claim 11, the invention relates to a video signal processing integrated circuit (IC), including a method for designing a de-emphasis circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the number of components of external application circuits of a de-emphasis output terminal of the video signal processing IC, and an IC made by the method.

The closest references Nonaka et al (US 5,872,605) disclose a video signal processing apparatus, which includes an equalizer for delaying an input color signal by an adjustable phase retardation, made into an integrated circuit, and Kitamura et al (US 5,132,806) teach semiconductor integrated circuit devices, including techniques which are effective when applied to a semiconductor integrated circuit device for use in a color video tape recorder (VTR).

However, Nonaka et al and Kitamura et al fail to explicitly disclose a method of designing a video signal processing integrated circuit (IC), where the method further

comprising the steps of incorporating a determining circuit for determining a level of a reproduced video signal of a de-emphasis circuit into the video signal processing IC, and connecting the determining circuit between an output of the de-emphasis circuit and a ground exclusively used for the luminance signal processing block.

Regarding claim 17, the invention relates to a video signal processing integrated circuit (IC), including a method for designing a de-emphasis circuit for a video signal processing IC in order to reduce operating steps and material costs by minimizing the number of components of external application circuits of a de-emphasis output terminal of the video signal processing IC, and an IC made by the method.

The closest references Nonaka et al (US 5,872,605) disclose a video signal processing apparatus, which includes an equalizer for delaying an input color signal by an adjustable phase retardation, made into an integrated circuit, and Kitamura et al (US 5,132,806) teach semiconductor integrated circuit devices, including techniques which are effective when applied to a semiconductor integrated circuit device for use in a color video tape recorder (VTR).

However, Nonaka et al and Kitamura et al fail to explicitly disclose a video signal processing circuit, where the circuit incorporates a determining circuit for determining a level of a reproduced video signal of a de-emphasis circuit, and a video level setting unit connected between the output of the de-emphasis circuit and a ground which is used exclusively for luminance signal processing.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamamoto et al (US 5,323,242) teach a video signal recording/reproducing apparatus such as a color video tape recorder (VTR), including a generator device for a carrier signal necessary for frequency conversion of a color signal of a VTR, a luminance signal processing device and a color signal processing device.

Christopher et al (US 4,286,282) teach video disc players, including video signal correction servo systems for such players.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Onuaku whose telephone number is 571-272-7379. The examiner can normally be reached on M-F.

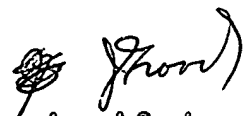
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached on 571-272-7950. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2621

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
COO

6/22/06

  
**James J. Groody**  
**Supervisory Patent Examiner**  
**Art Unit 262-2621**